



# VNB14NV04/VND14NV04 VND14NV04-1/VNP14NV04/VNS14NV04

## “OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

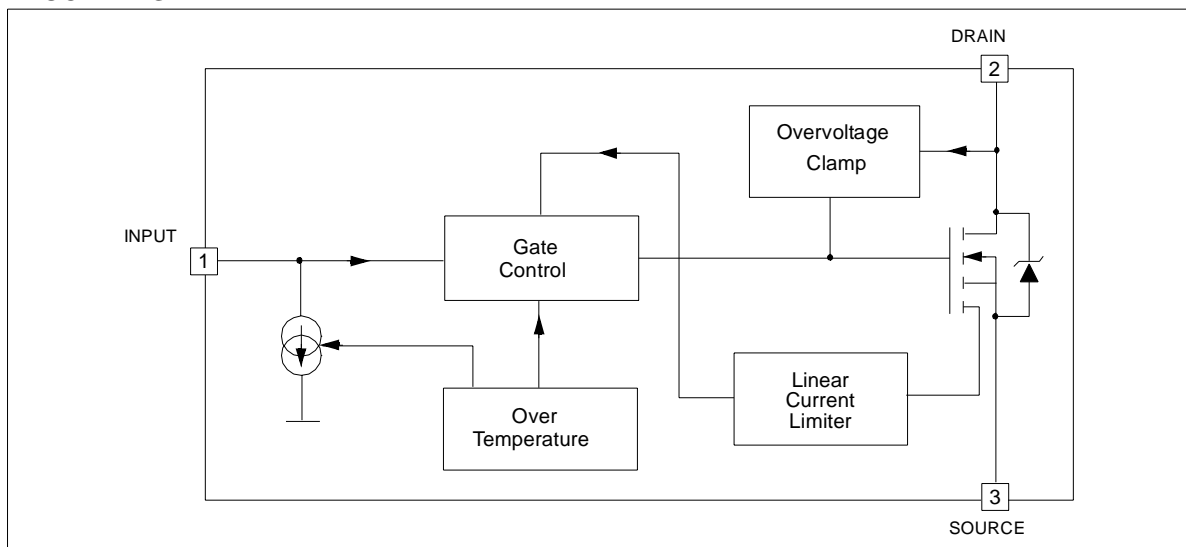
TYPE	$R_{DS(on)}$	$I_{lim}$	$V_{clamp}$
VNB14NV04	35 mΩ	12 A	40 V
VND14NV04			
VND14NV04-1			
VNP14NV04			
VNS14NV04			


- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

### DESCRIPTION


The VNB14NV04, VND14NV04, VND14NV04-1, VNP14NV04, VNS14NV04, are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETS from DC up to 50KHz

### BLOCK DIAGRAM






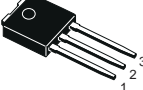
TO-252 (DPAK)



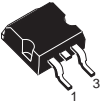
SO-8



TO-220



TO-251 (IPAK)



D<sup>2</sup>PAK

ORDER CODES		
PACKAGE	TUBE	T&R
D <sup>2</sup> PAK	VNB14NV04	VNB14NV0413TR
TO-252 (DPAK)	VND14NV04	VND14NV0413TR
TO-251 (IPAK)	VND14NV04-1	-
TO-220	VNP14NV04	-
SO-8	VNS14NV04	-

applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

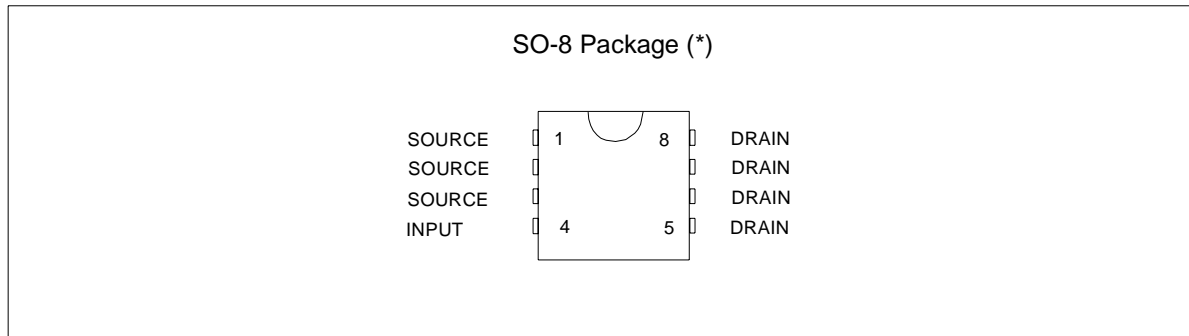
Fault feedback can be detected by monitoring the voltage at the input pin.

## VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

### ABSOLUTE MAXIMUM RATING

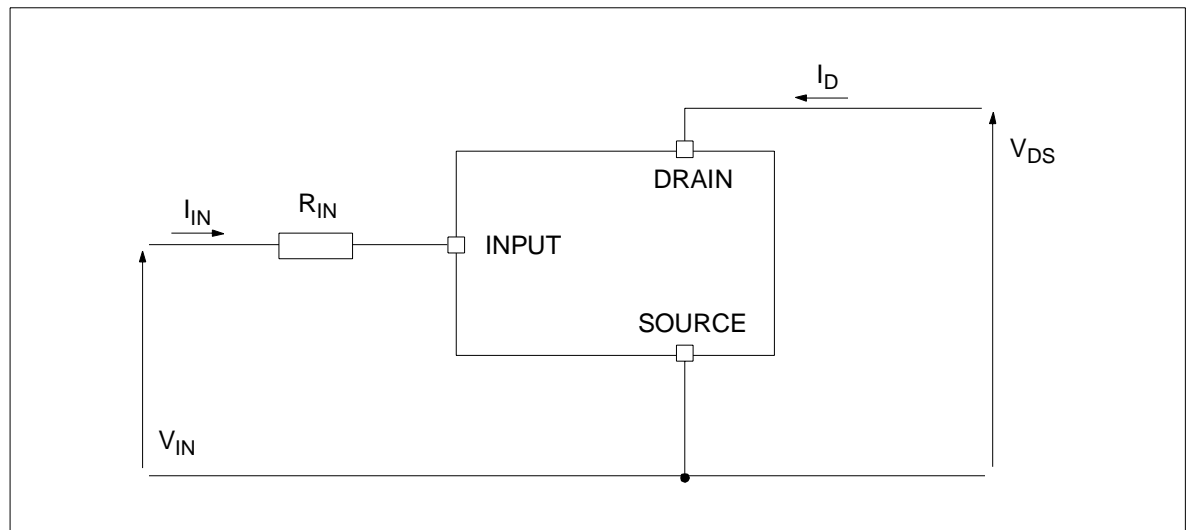
Symbol	Parameter	Value					Unit
		SO-8	DPAK	TO-220	IPAK	D <sup>2</sup> PAK	
$V_{DS}$	Drain-source Voltage ( $V_{IN}=0V$ )	Internally Clamped					V
$V_{IN}$	Input Voltage	Internally Clamped					V
$I_{IN}$	Input Current	+/-20					mA
$R_{IN\ MIN}$	Minimum Input Series Impedance	10					$\Omega$
$I_D$	Drain Current	Internally Limited					A
$I_R$	Reverse DC Output Current	-15					A
$V_{ESD1}$	Electrostatic Discharge ( $R=1.5K\Omega$ , $C=100pF$ )	4000					V
$V_{ESD2}$	Electrostatic Discharge on output pin only ( $R=330\Omega$ , $C=150pF$ )	16500					V
$P_{tot}$	Total Dissipation at $T_c=25^\circ C$	4.6	74	74	74	74	W
$E_{MAX}$	Maximum Switching Energy ( $L=0.4mH$ ; $R_L=0\Omega$ ; $V_{bat}=13.5V$ ; $T_{j\ start}=150^\circ C$ ; $I_L=18A$ )		93			93	mJ
$T_j$	Operating Junction Temperature	Internally limited					$^\circ C$
$T_c$	Case Operating Temperature	Internally limited					$^\circ C$
$T_{stg}$	Storage Temperature	-55 to 150					$^\circ C$

### CONNECTION DIAGRAM (TOP VIEW)



(\*) For the pins configuration related to DPAK, D<sup>2</sup>PAK, IPA, TO-220 see outlines at page 1.

### CURRENT AND VOLTAGE CONVENTIONS



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

**THERMAL DATA**

Symbol	Parameter	Value					Unit
		SO-8	DPAK	TO-220	IPAK	D <sup>2</sup> PAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case MAX		1.7	1.7	1.7	1.7	°C/W
R <sub>thj-lead</sub>	Thermal Resistance Junction-lead MAX	27					°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient MAX	90 (*)	65 (*)	62	102	52 (*)	°C/W

(\*) When mounted on a standard single-sided FR4 board with 0.5cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all DRAIN pins. Horizontal mounting and no artificial air flow.

**ELECTRICAL CHARACTERISTICS** (-40°C < T<sub>j</sub> < 150°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CLAMP</sub>	Drain-source Clamp Voltage	V <sub>IN</sub> =0V; I <sub>D</sub> =7A	40	45	55	V
V <sub>CLTH</sub>	Drain-source Clamp Threshold Voltage	V <sub>IN</sub> =0V; I <sub>D</sub> =2mA	36			V
V <sub>INTH</sub>	Input Threshold Voltage	V <sub>DS</sub> =V <sub>IN</sub> ; I <sub>D</sub> =1mA	0.5		2.5	V
I <sub>ISS</sub>	Supply Current from Input Pin	V <sub>DS</sub> =0V; V <sub>IN</sub> =5V		100	150	μA
V <sub>INCL</sub>	Input-Source Clamp Voltage	I <sub>IN</sub> =1mA I <sub>IN</sub> =-1mA	6 -1.0	6.8	8 -0.3	V
I <sub>DSS</sub>	Zero Input Voltage Drain Current (V <sub>IN</sub> =0V)	V <sub>DS</sub> =13V; V <sub>IN</sub> =0V; T <sub>j</sub> =25°C V <sub>DS</sub> =25V; V <sub>IN</sub> =0V			30 75	μA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>IN</sub> =5V; I <sub>D</sub> =7A; T <sub>j</sub> =25°C V <sub>IN</sub> =5V; I <sub>D</sub> =7A			35 70	mΩ

## VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

### ELECTRICAL CHARACTERISTICS (continued) ( $T_j=25^\circ\text{C}$ , unless otherwise specified)

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$g_{fs}^*$	Forward Transconductance	$V_{DD}=13\text{V}; I_D=7\text{A}$		18		S
$C_{OSS}$	Output Capacitance	$V_{DS}=13\text{V}; f=1\text{MHz}; V_{IN}=0\text{V}$		400		pF

#### SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=7\text{A}$		80	250	ns
$t_r$	Rise Time			350	1000	ns
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=R_{IN\ MIN}=10\Omega$ (see figure 1)		450	1350	ns
$t_f$	Fall Time			150	500	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=7\text{A}$		1.5	4.5	$\mu\text{s}$
$t_r$	Rise Time			9.7	30.0	$\mu\text{s}$
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=2.2\text{K}\Omega$ (see figure 1)		9	25.0	$\mu\text{s}$
$t_f$	Fall Time			10.2	30.0	$\mu\text{s}$
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}; I_D=7\text{A}$ $V_{gen}=5\text{V}; R_{gen}=R_{IN\ MIN}=10\Omega$		16		$\text{A}/\mu\text{s}$
$Q_i$	Total Input Charge	$V_{DD}=12\text{V}; I_D=7\text{A}; V_{IN}=5\text{V}; I_{gen}=2.13\text{mA}$ (see figure 5)		36.8		nC

#### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD}^*$	Forward On Voltage	$I_{SD}=7\text{A}; V_{IN}=0\text{V}$		0.8		V
$t_{rr}$	Reverse Recovery Time	$I_{SD}=7\text{A}; di/dt=40\text{A}/\mu\text{s}$		300		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD}=30\text{V}; L=200\mu\text{H}$		0.8		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current	(see test circuit, figure 2)		5		A

#### PROTECTIONS ( $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{lim}$	Drain Current Limit	$V_{IN}=5\text{V}; V_{DS}=13\text{V}$	12	18	24	A
$t_{dim}$	Step Response Current Limit	$V_{IN}=5\text{V}; V_{DS}=13\text{V}$		45		$\mu\text{s}$
$T_{jsh}$	Overtemperature Shutdown		150	175	200	$^\circ\text{C}$
$T_{jrs}$	Overtemperature Reset		135			$^\circ\text{C}$
$I_{gf}$	Fault Sink Current	$V_{IN}=5\text{V}; V_{DS}=13\text{V}; T_j=T_{jsh}$	10	15	20	mA
$E_{as}$	Single Pulse Avalanche Energy	starting $T_j=25^\circ\text{C}; V_{DD}=24\text{V}$ $V_{IN}=5\text{V}; R_{gen}=R_{IN\ MIN}=10\Omega; L=24\text{mH}$ (see figures 3 & 4)	400			mJ

(\*) Pulsed: Pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50KHz. The only difference from the user's standpoint is that a small DC current  $I_{SS}$  (typ. 100 $\mu$ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

### - OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

### - LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current  $I_D$  to  $I_{lim}$  whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold  $T_{jsh}$ .

### - OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

### - STATUS FEEDBACK:

in the case of an overtemperature fault condition ( $T_j > T_{jsh}$ ), the device tries to sink a diagnostic current  $I_{gf}$  through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current  $I_{gf}$ , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current  $I_{SS}$ .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 1: Switching Time Test Circuit for Resistive Load

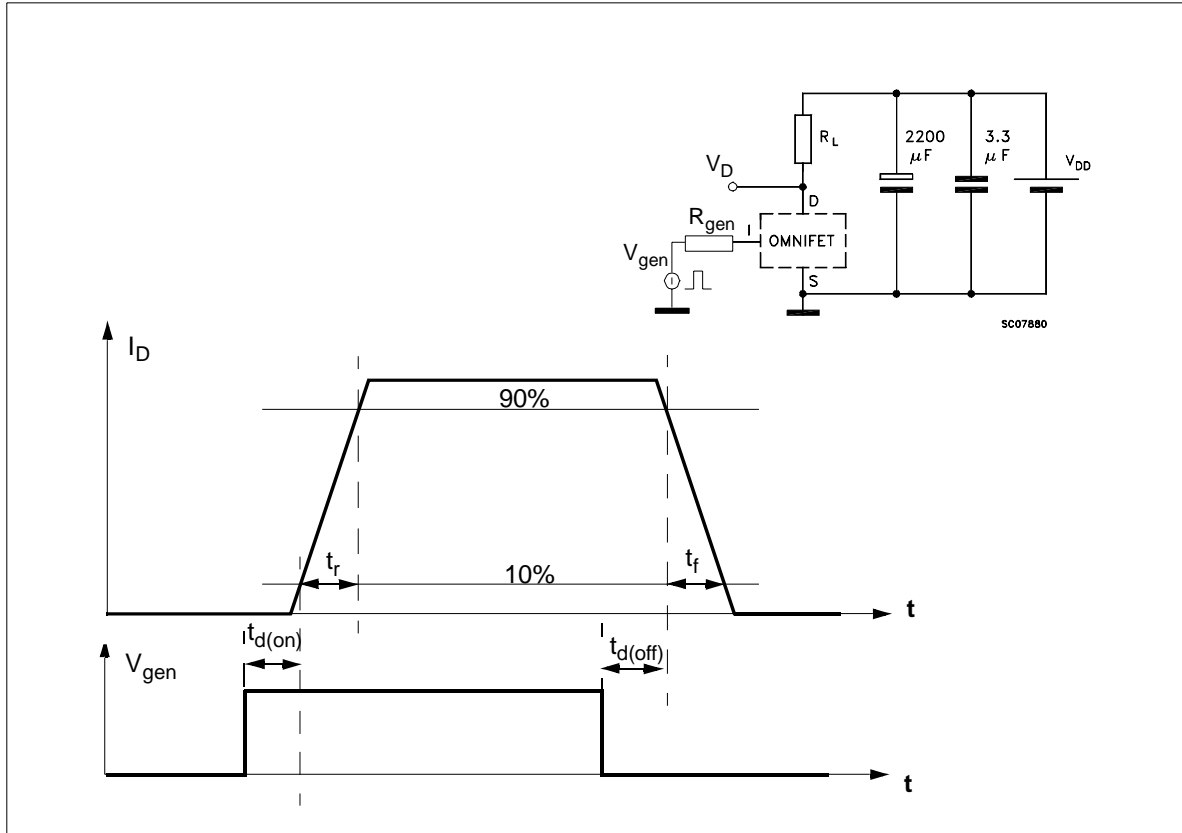


Figure 2: Test Circuit for Diode Recovery Times

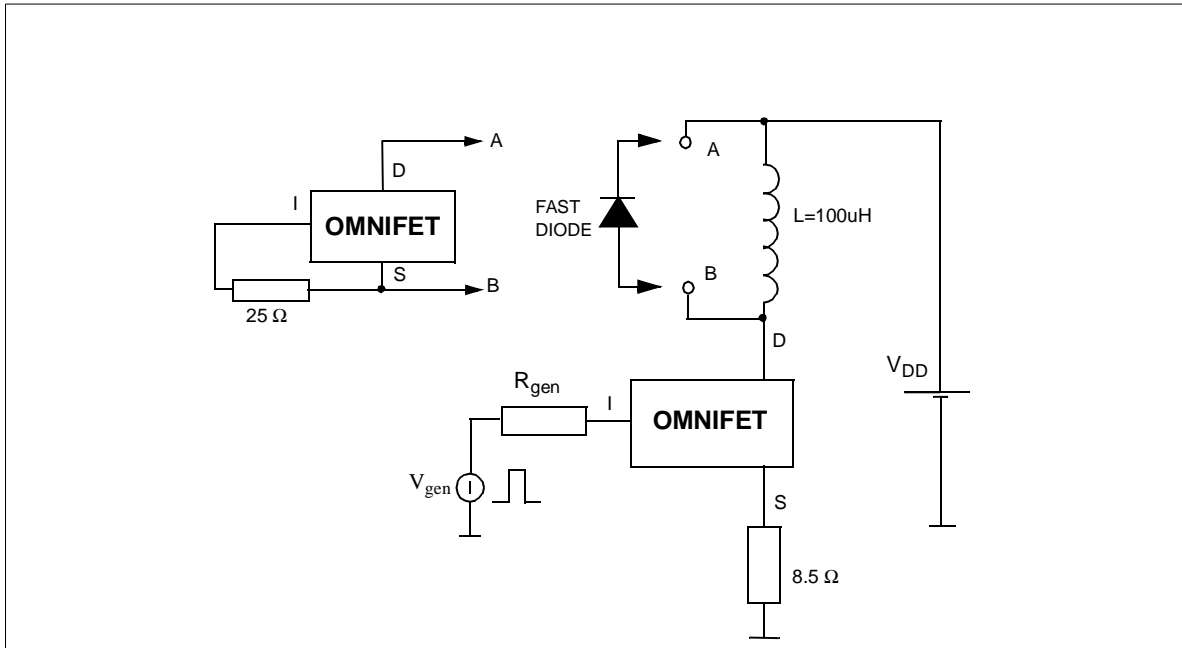


Figure 3: Unclamped Inductive Load Test Circuits

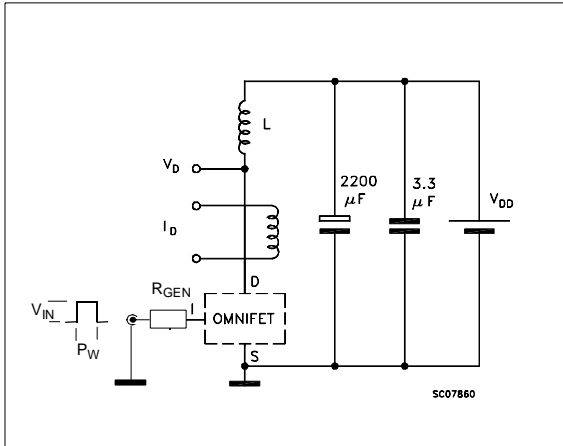


Figure 4: Unclamped Inductive Waveforms

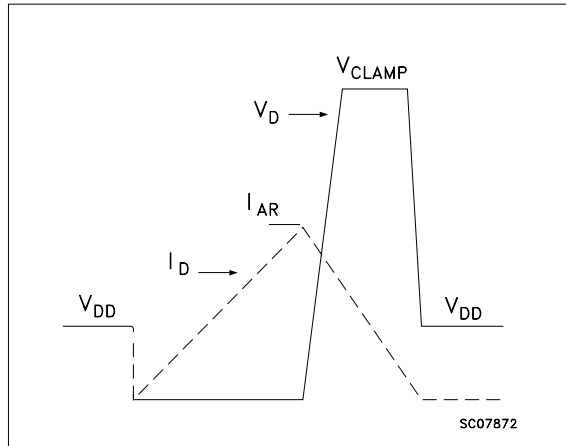
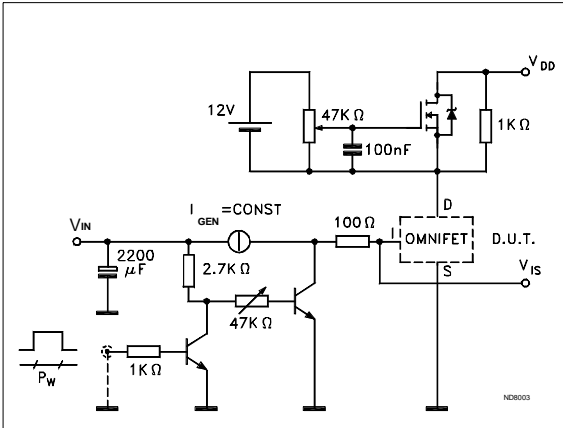
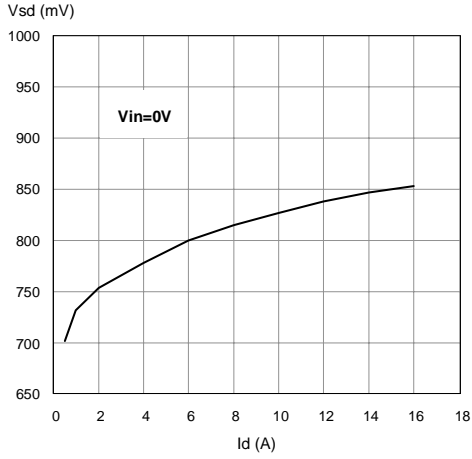


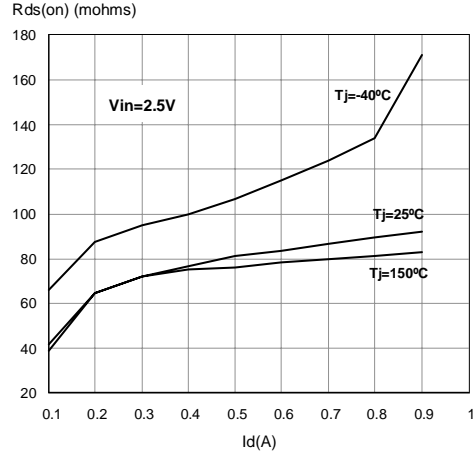
Figure 5: Input Charge Test Circuit



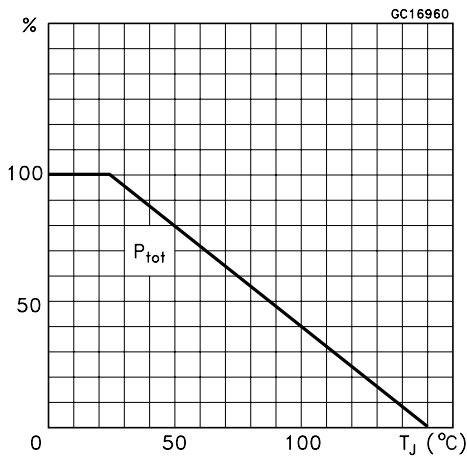
Source-Drain Diode Forward Characteristics



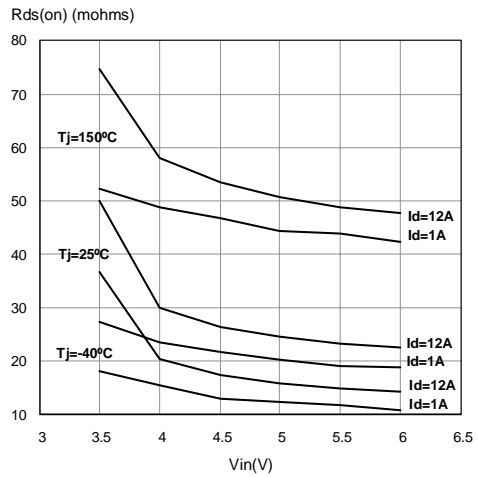
Static Drain Source On Resistance



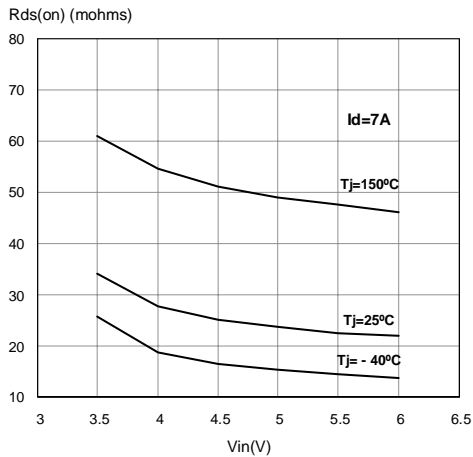
Derating Curve



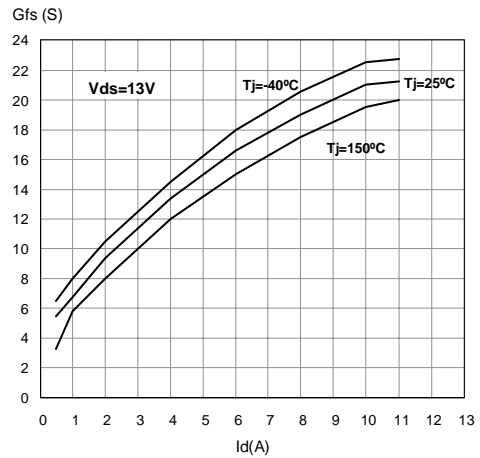
Static Drain-Source On resistance Vs. Input Voltage



Static Drain-Source On resistance Vs. Input Voltage

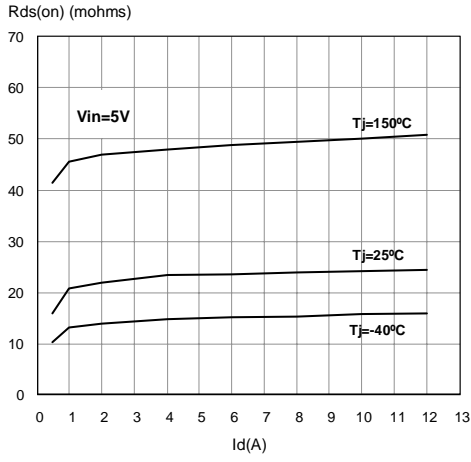


Transconductance

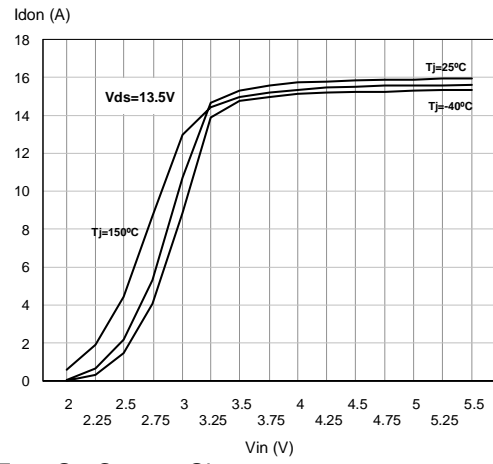




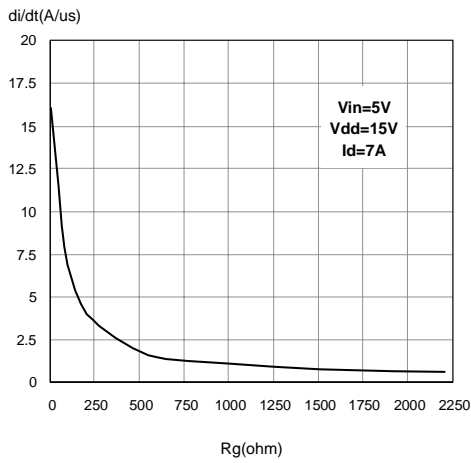
Static Drain-Source On Resistance Vs. Id



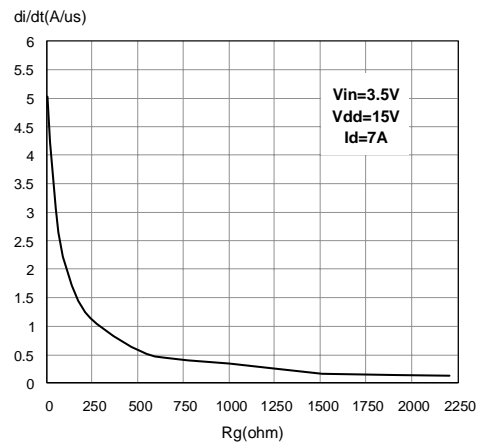
Transfer Characteristics



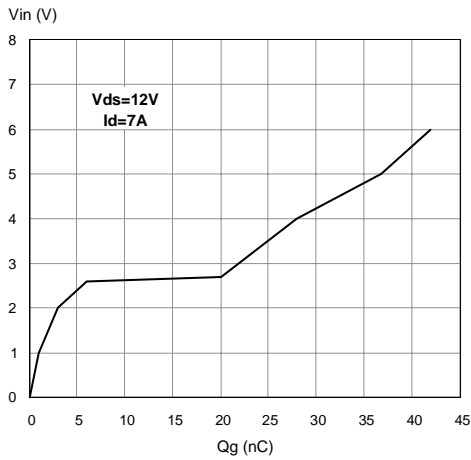
Turn On Current Slope



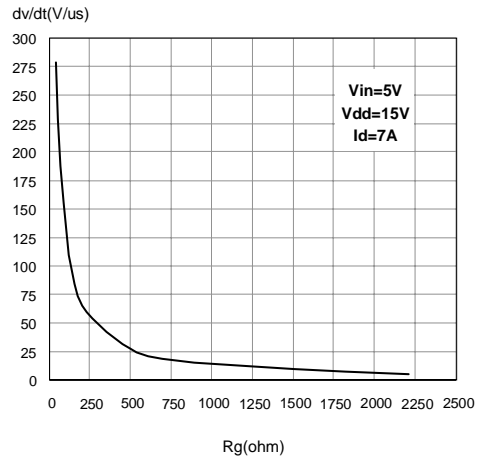
Turn On Current Slope



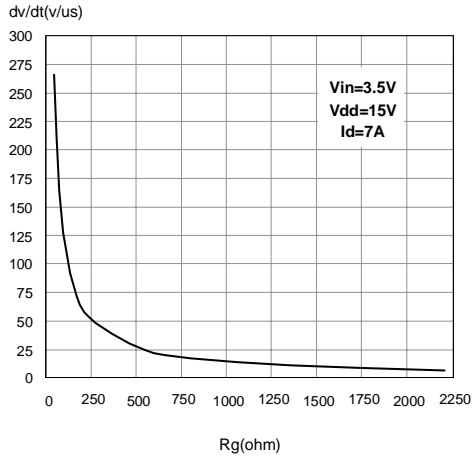
Input Voltage Vs. Input Charge



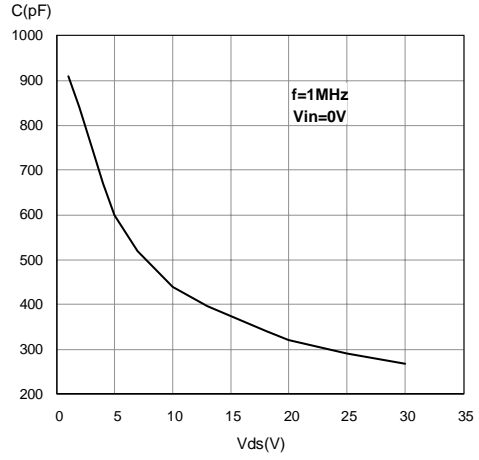
Turn off drain source voltage slope



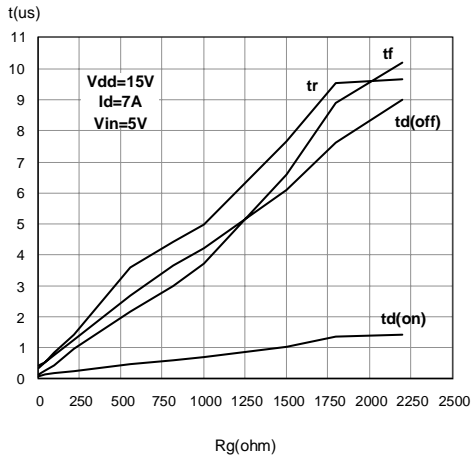
Turn Off Drain-Source Voltage Slope



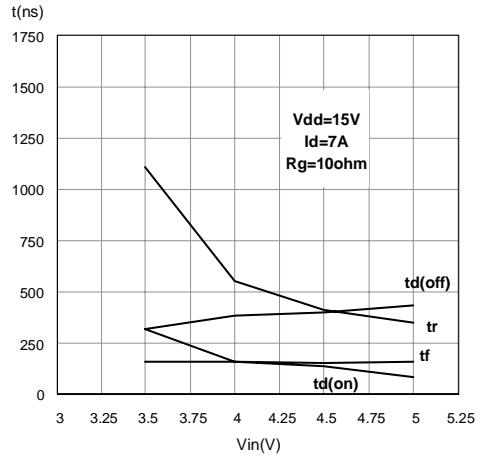
Capacitance Variations



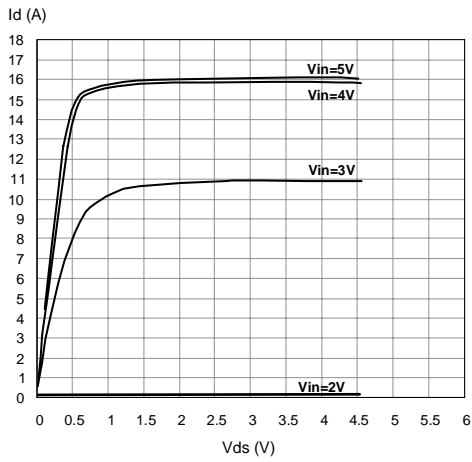
Switching Time Resistive Load



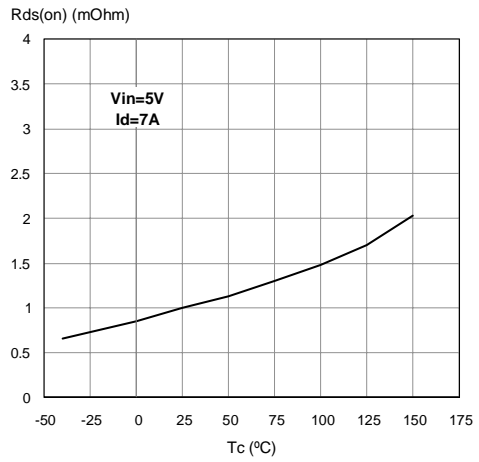
Switching Time Resistive Load



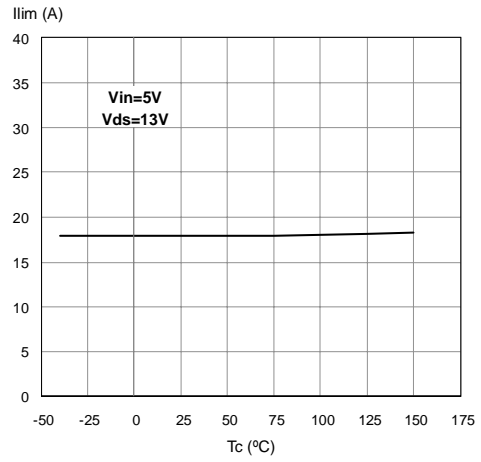
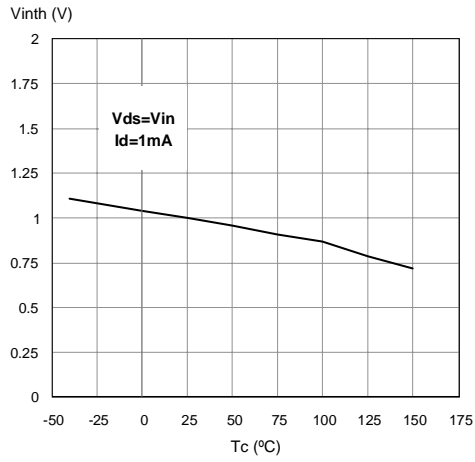
Output Characteristics



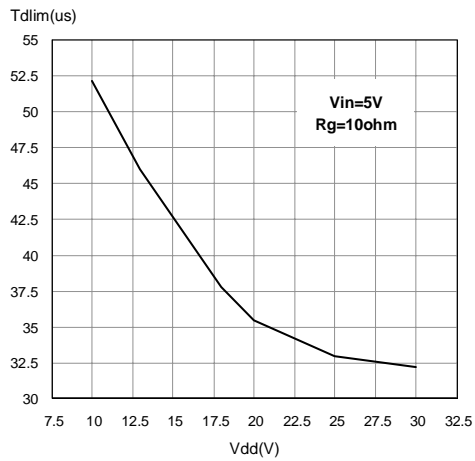
Normalized On Resistance Vs. Temperature



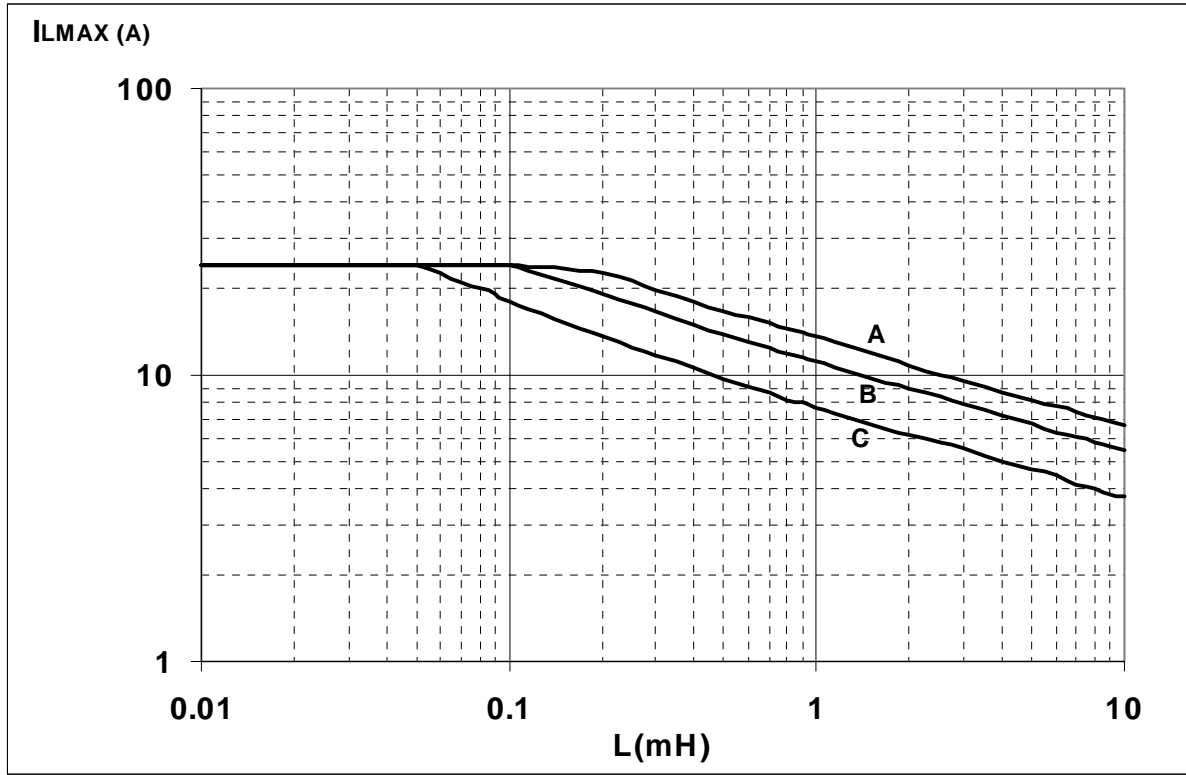
Normalized Input Threshold Voltage Vs. Current Limit Vs. Junction Temperature



Step Response Current Limit



DPAK Maximum turn off current versus load inductance



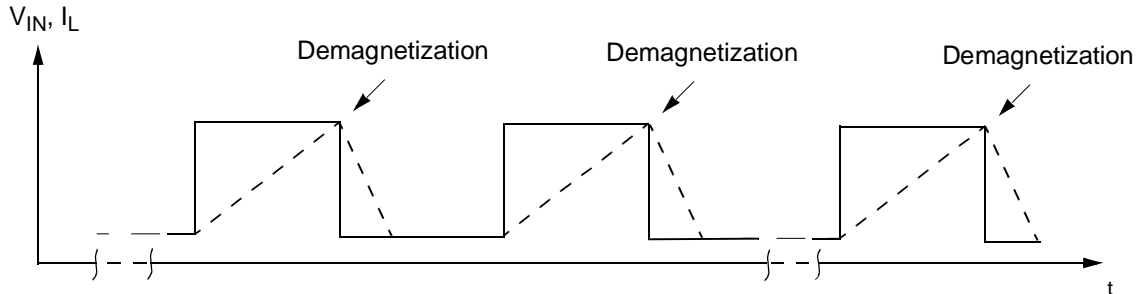
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

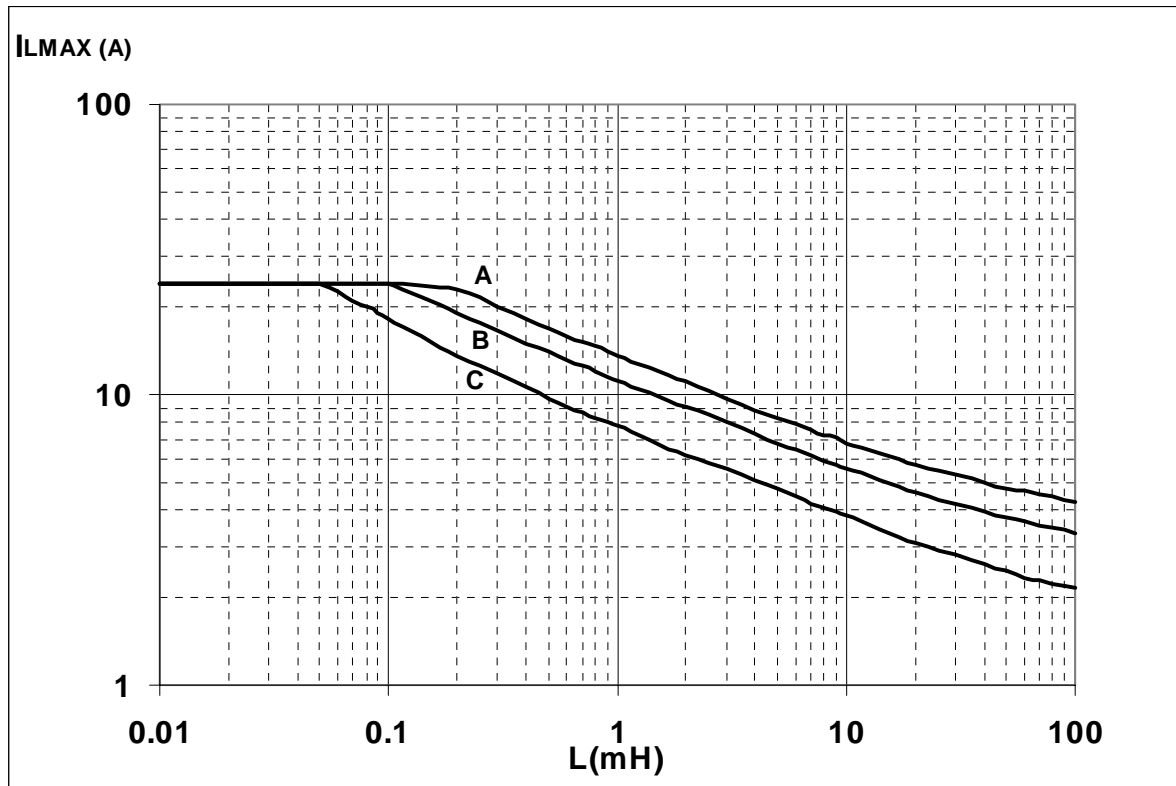
$V_{CC}=13.5V$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



D<sup>2</sup>PAK Maximum turn off current versus load inductance



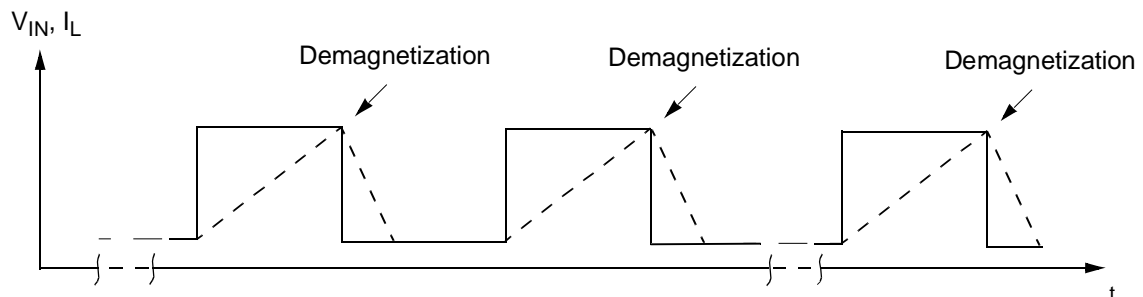
- A = Single Pulse at  $T_{jstart}=150^{\circ}C$
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- C = Repetitive Pulse at  $T_{jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

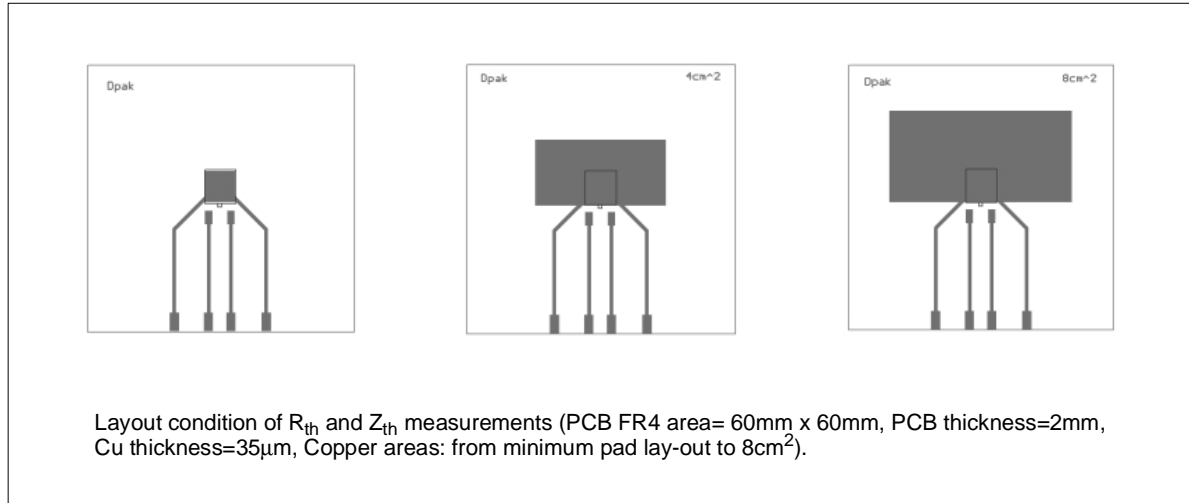
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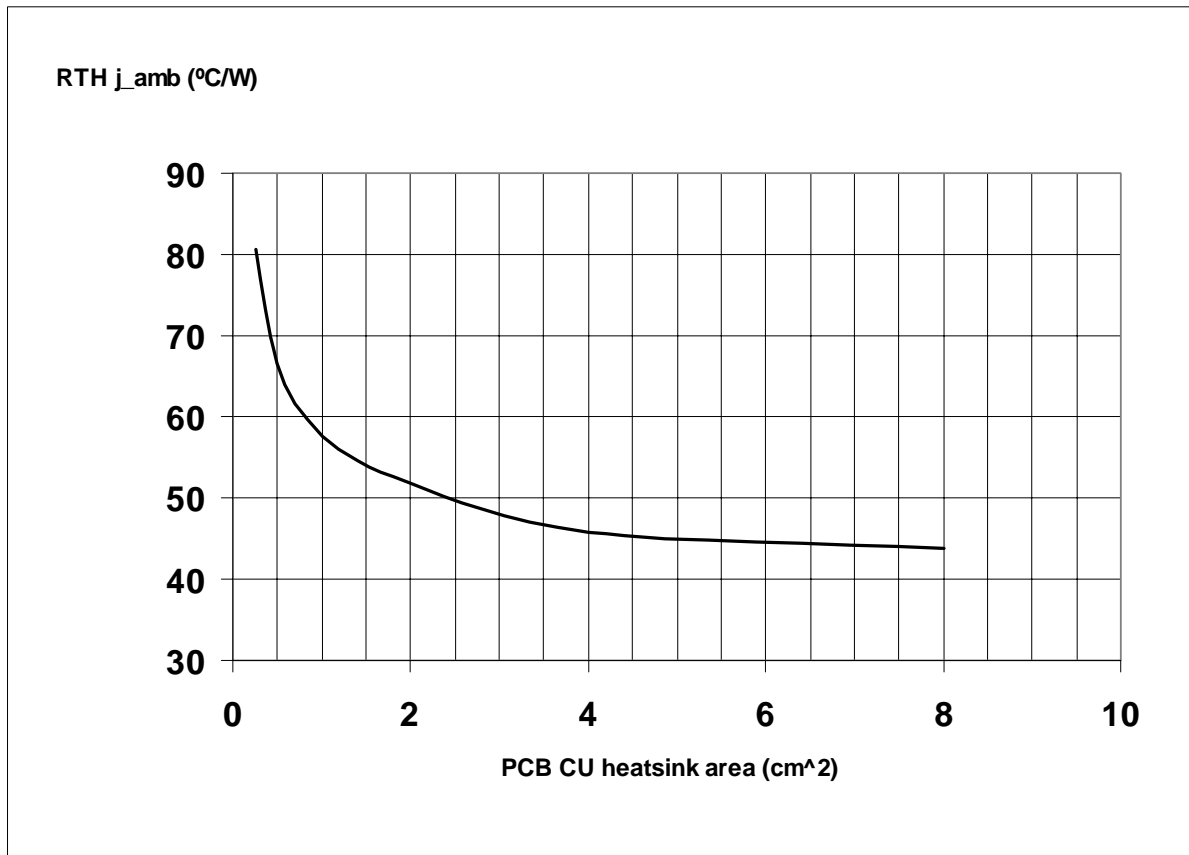


**DPAK THERMAL DATA**

**DPAK PC Board**




**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**




**SO-8 THERMAL DATA**

**SO-8 PC Board**


UNSxNU04      0.14cm<sup>2</sup>



UNSxNU04      0.6cm<sup>2</sup>

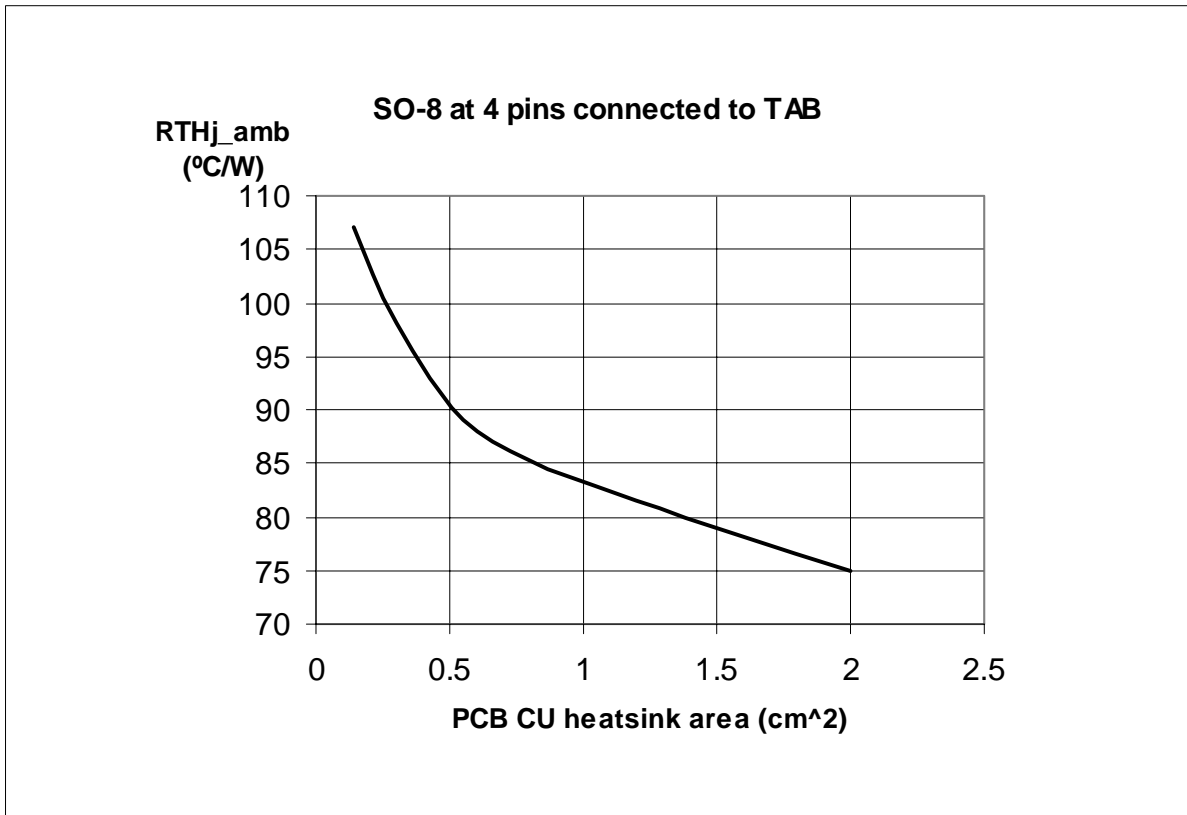


UNSxNU04      1.6cm<sup>2</sup>



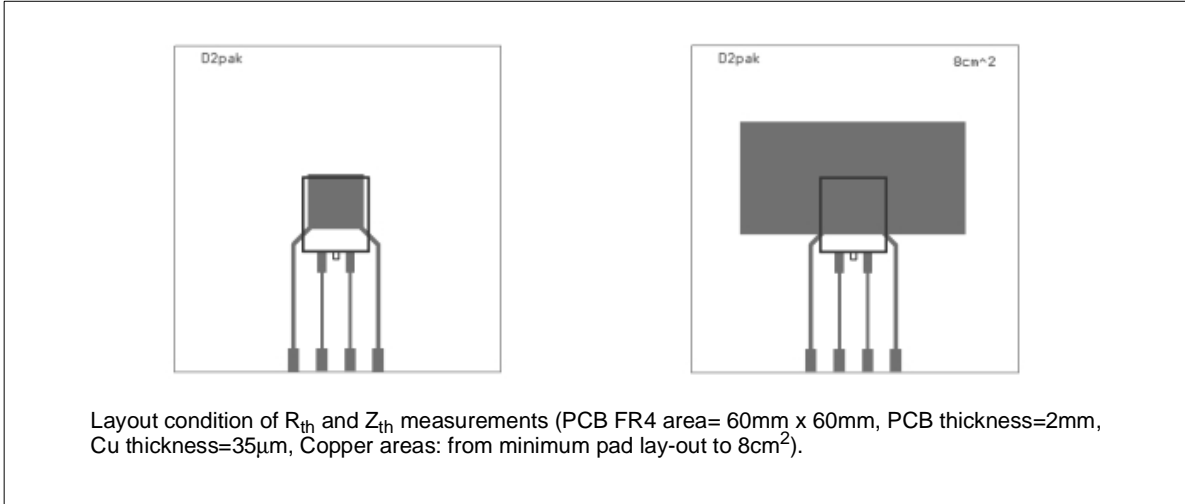
Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.14cm<sup>2</sup>, 0.6cm<sup>2</sup>, 1.6cm<sup>2</sup>).

**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**

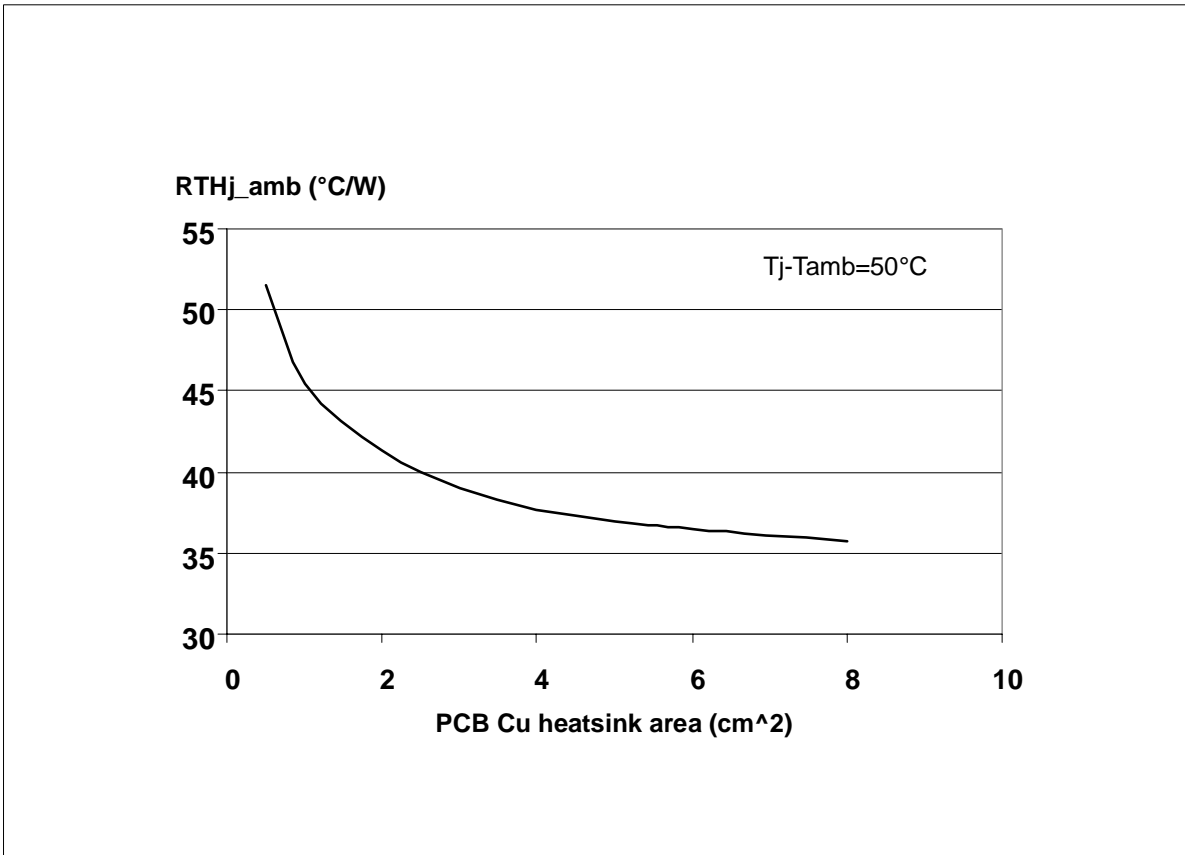


**D<sup>2</sup>PAK THERMAL DATA**

**D<sup>2</sup>PAK PC Board**

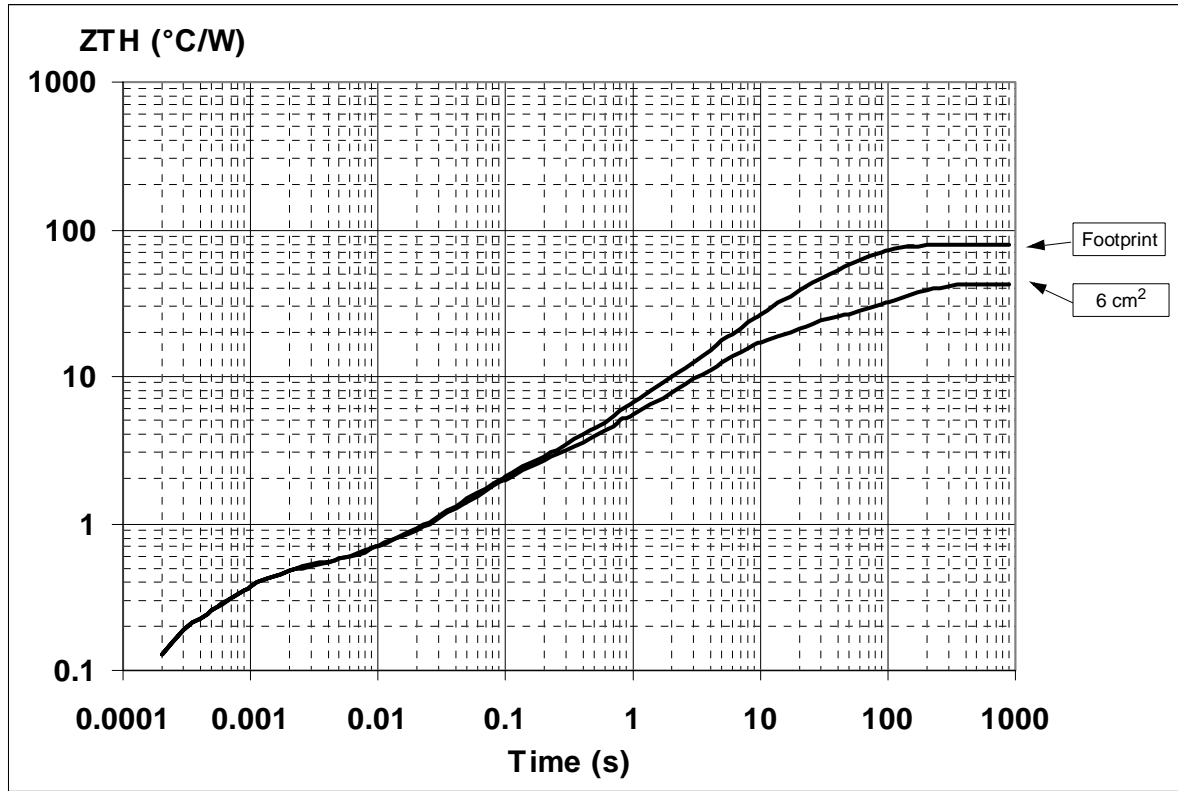


**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**

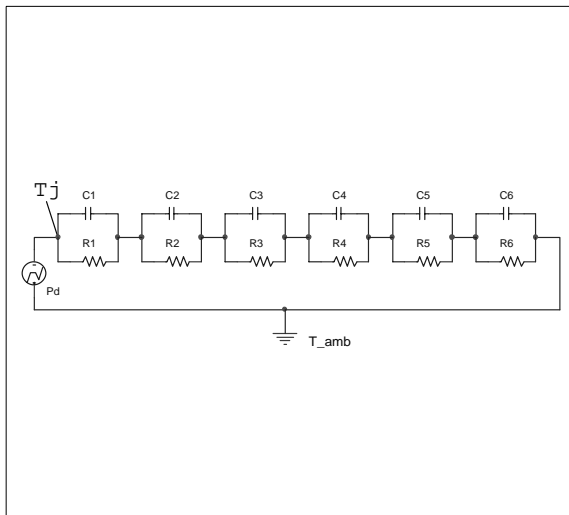




DPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

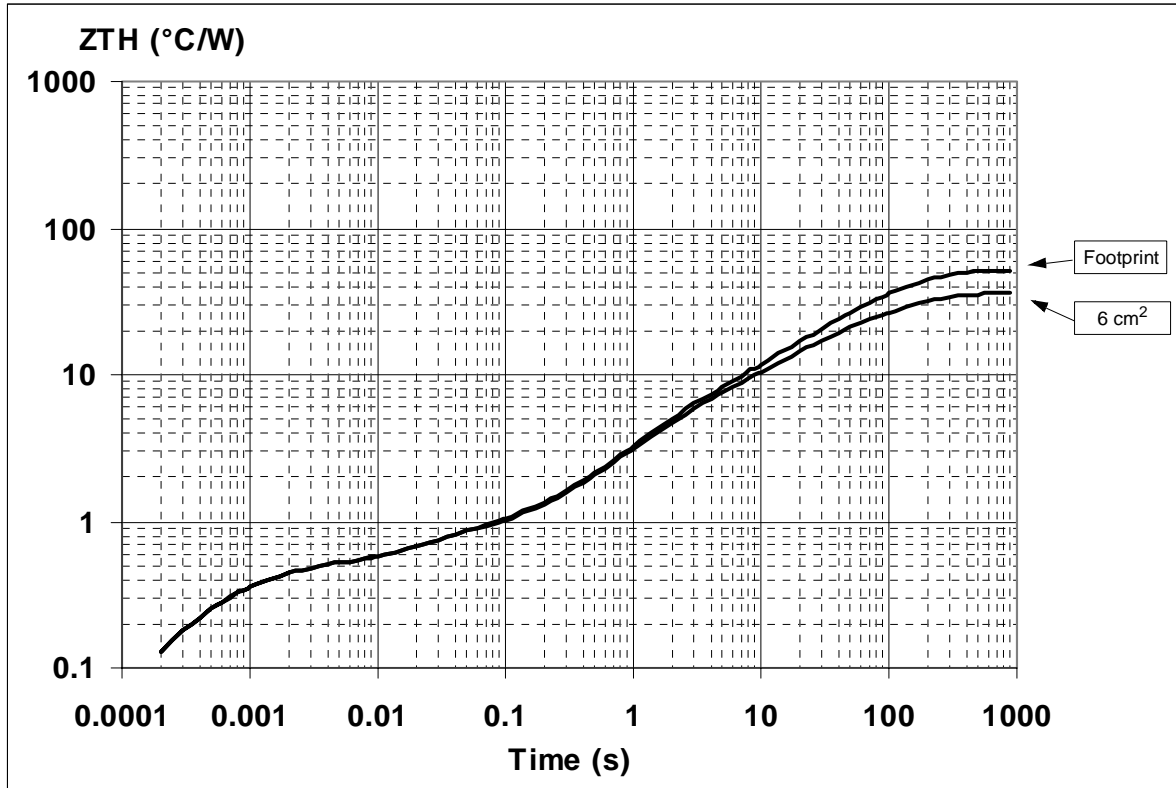
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

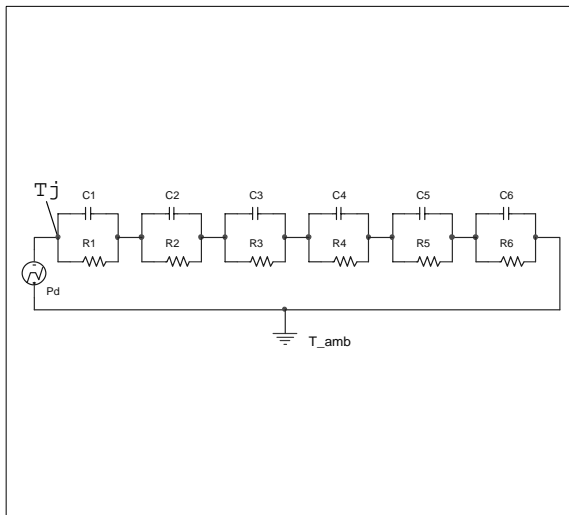
Thermal Parameter

Area/island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	1.20	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0021	
C3 (W.s/°C)	0.05	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

D<sup>2</sup>PAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in D<sup>2</sup>PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

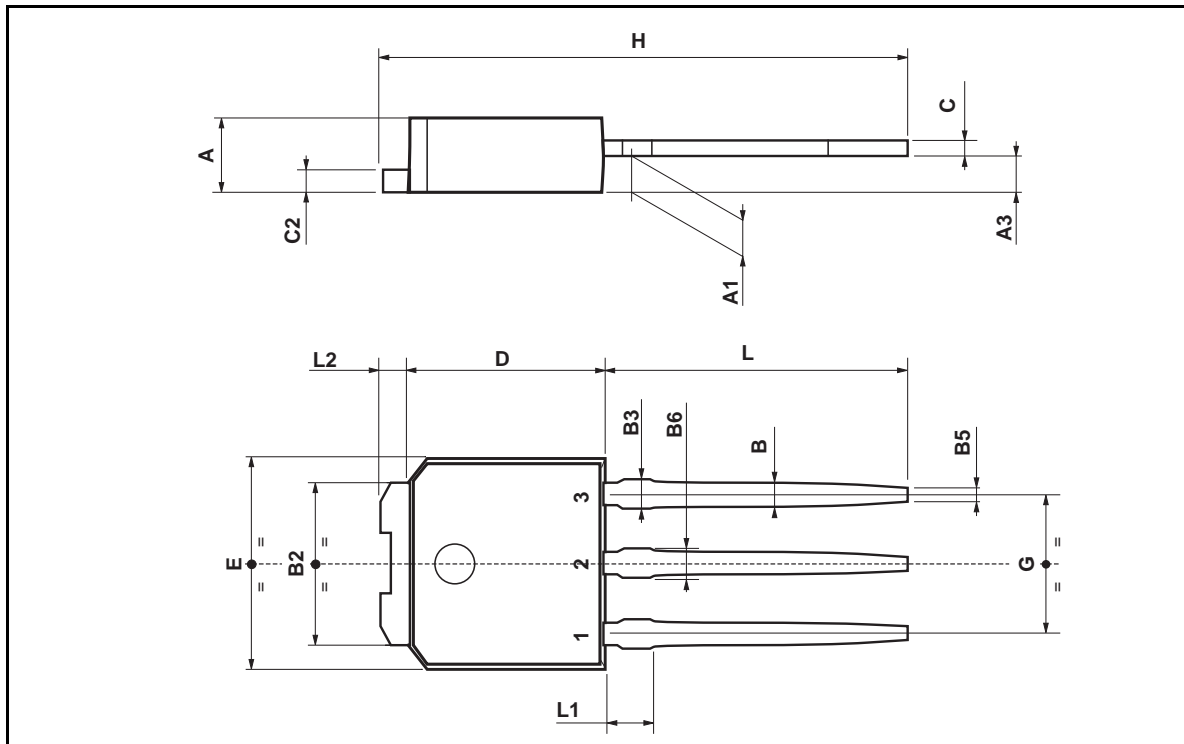
where  $\delta = t_p/T$

Thermal Parameter

Area/island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	
C3 (W.s/°C)	8.00E-02	
C4 (W.s/°C)	0.45	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

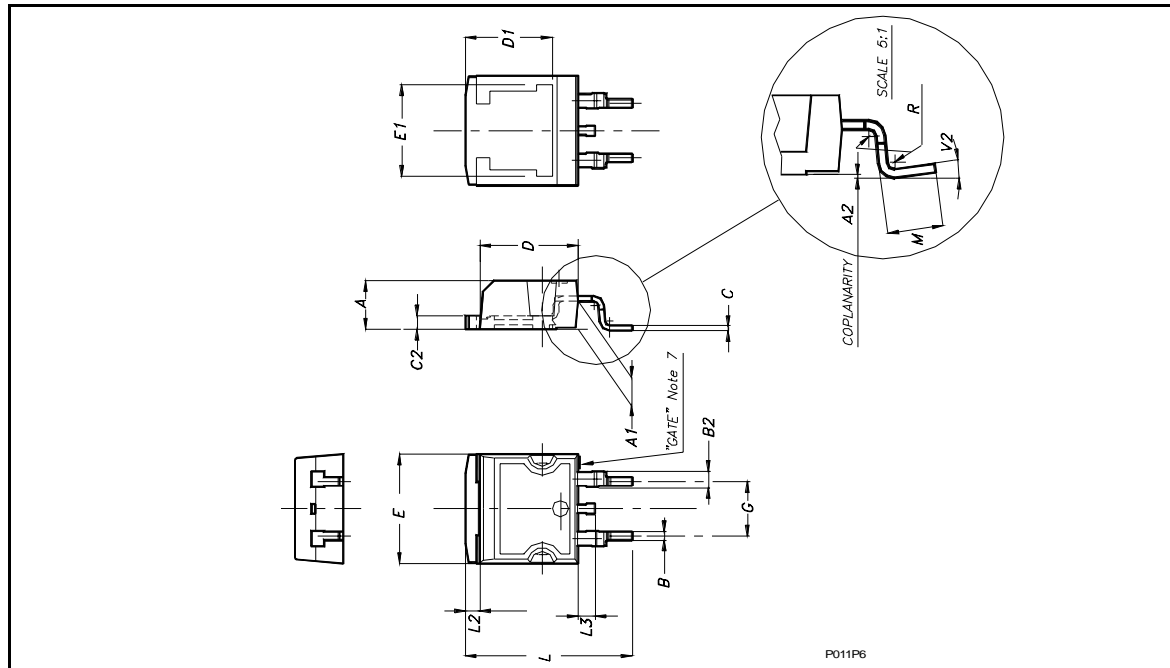
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



**D<sup>2</sup>PAK MECHANICAL DATA**

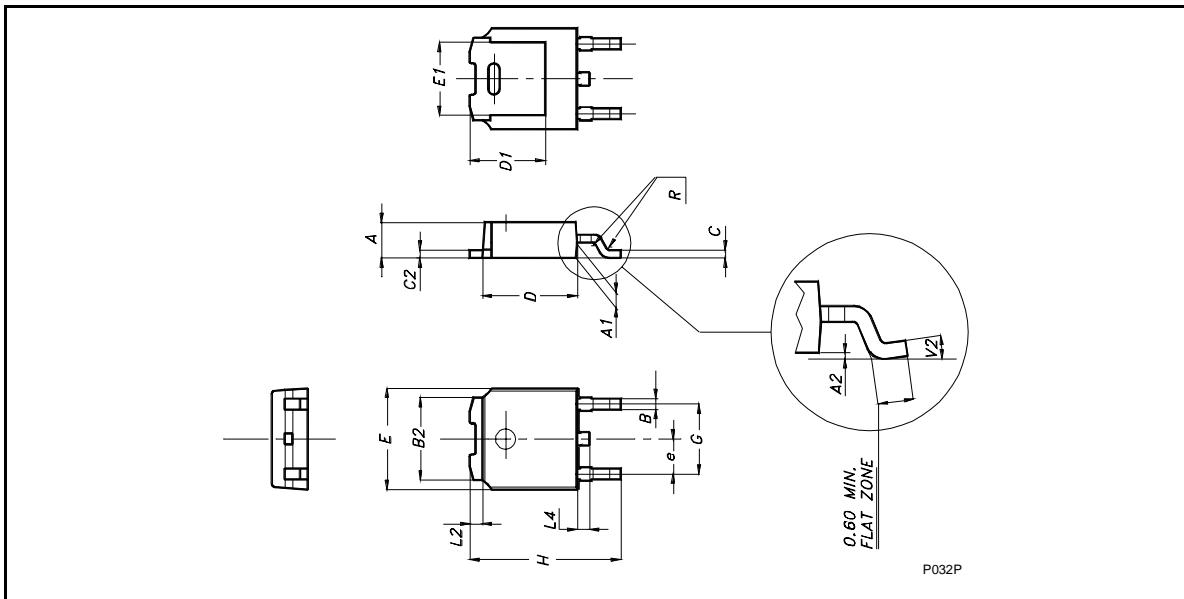
DIM.	mm.		
	MIN.	TYP	MAX.
A	4.4		4.6
A1	2.49		2.69
A2	0.03		0.23
B	0.7		0.93
B2	1.14		1.7
C	0.45		0.6
C2	1.23		1.36
D	8.95		9.35
D1		8	
E	10		10.4
E1		8.5	
G	4.88		5.28
L	15		15.85
L2	1.27		1.4
L3	1.4		1.75
M	2.4		3.2
R		0.4	
V2	0°		8°



P011P6

**TO-252 (DPAK) MECHANICAL DATA**

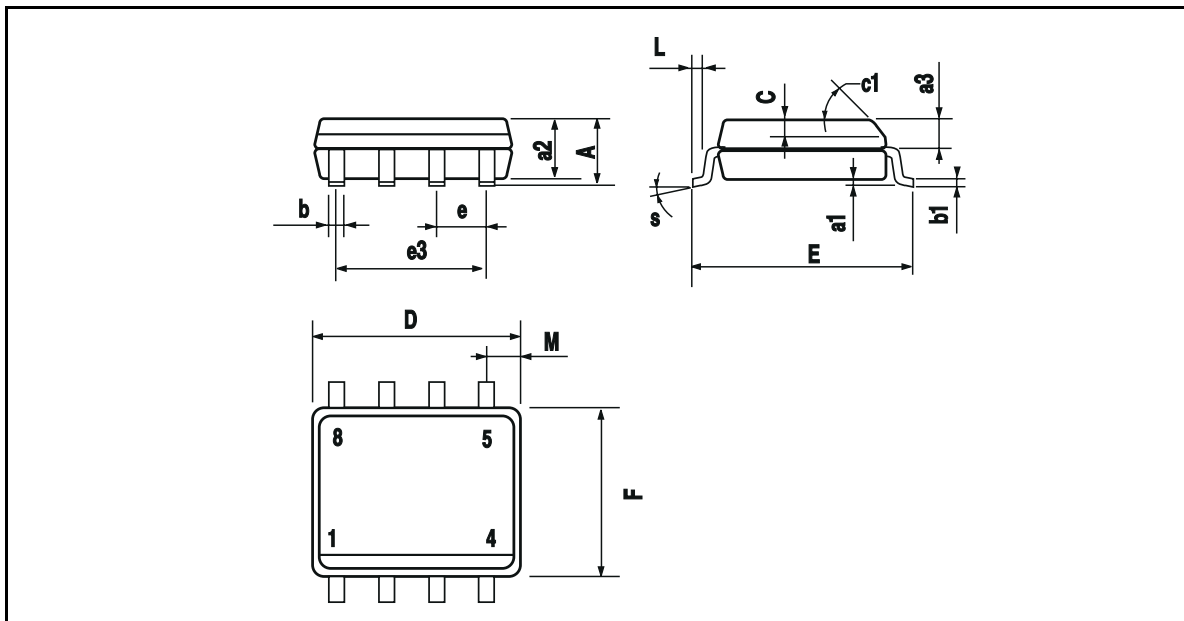
DIM.	mm.		
	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package Weight	Gr. 0.29		



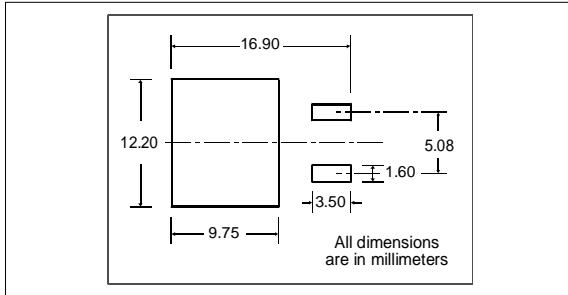


**SO-8 MECHANICAL DATA**

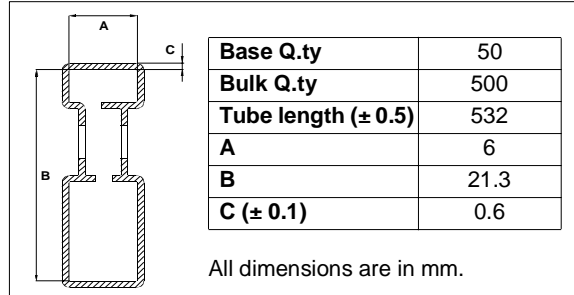
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
F	8 (max.)					



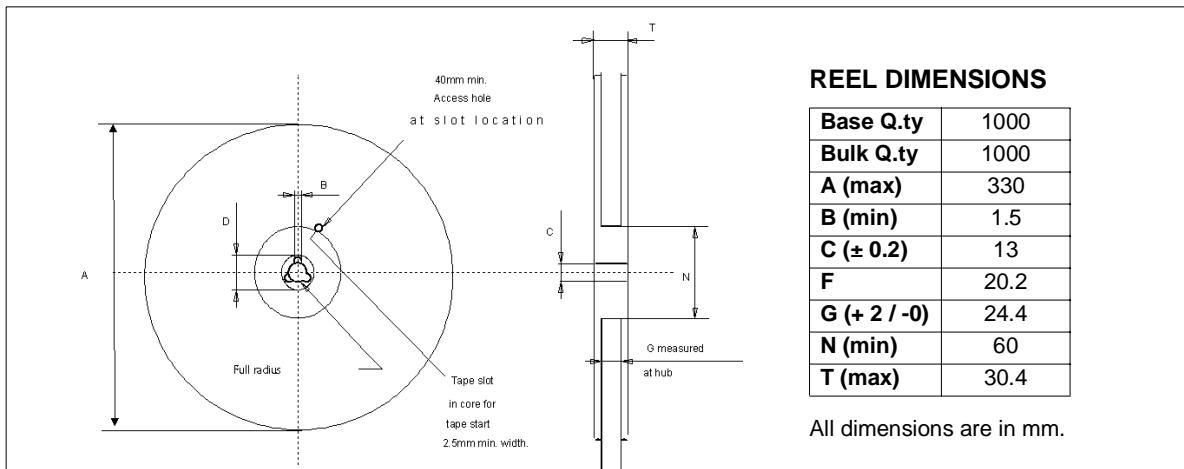
**D<sup>2</sup>PAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)**



**TAPE AND REEL SHIPMENT (suffix "13TR")**

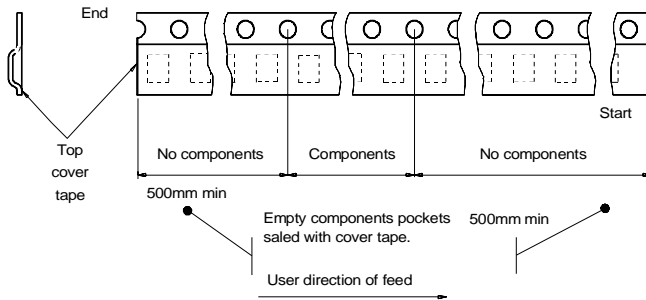
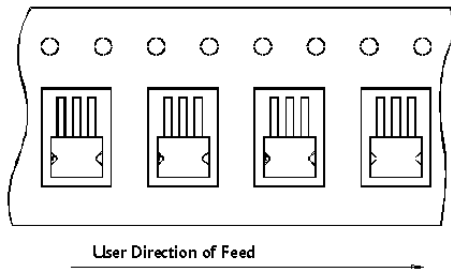
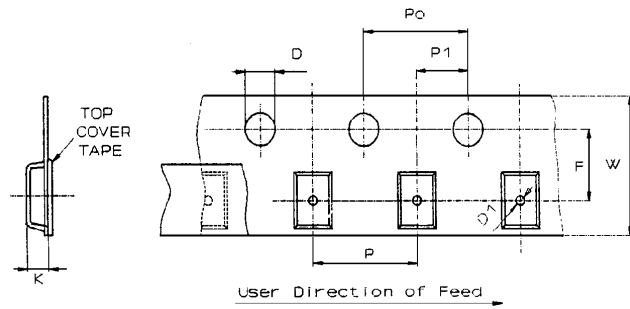


**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

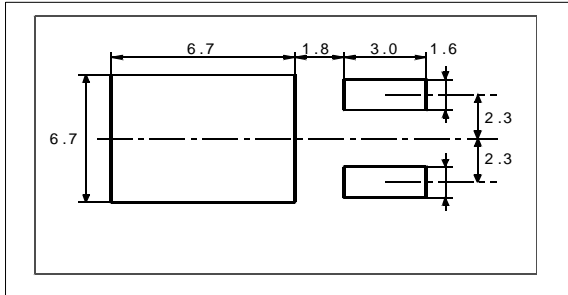
All dimensions are in mm.



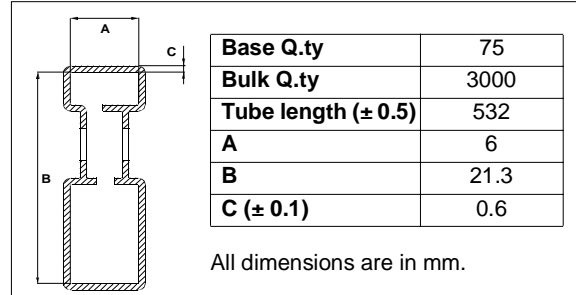


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

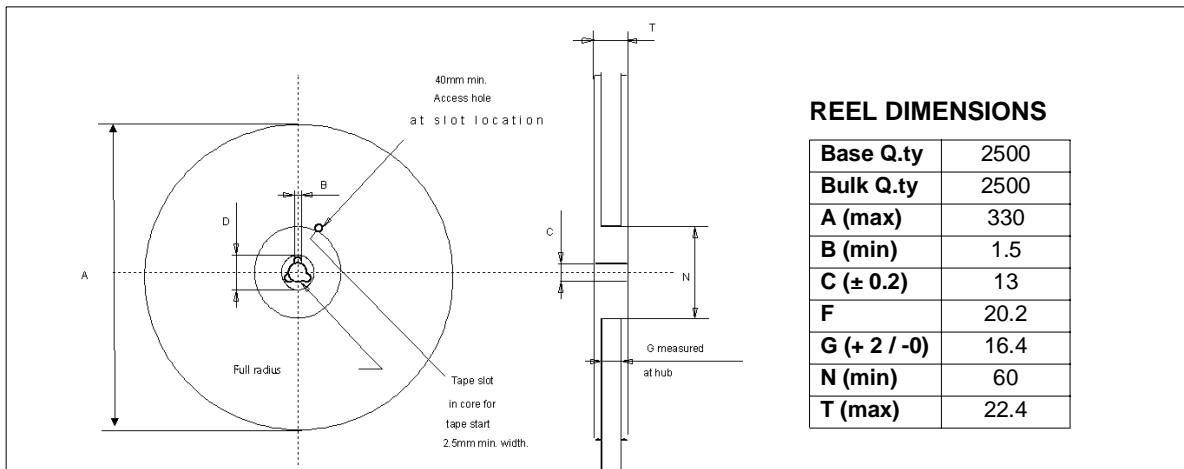
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

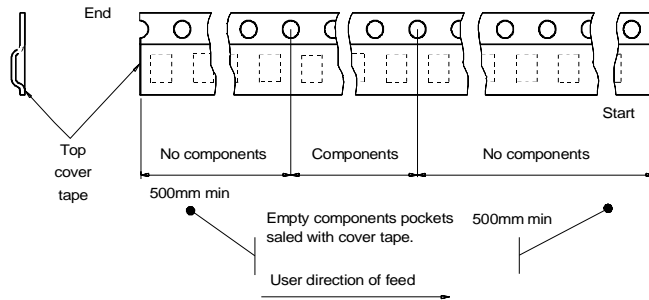
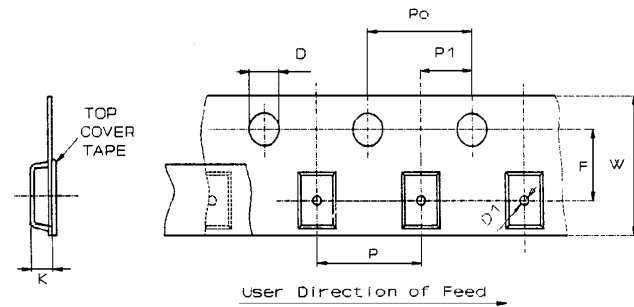
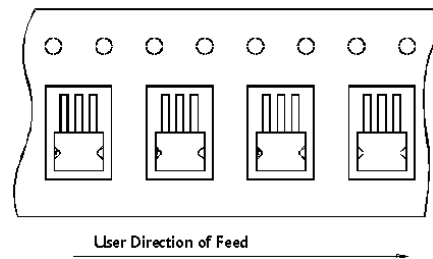


TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

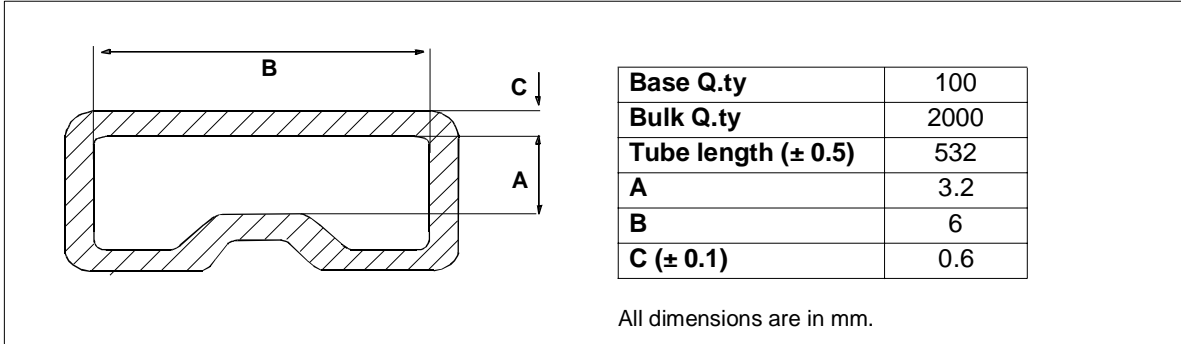
Tape width	W	16
Tape Hole Spacing	P0 ( $\pm 0.1$ )	4
Component Spacing	P	8
Hole Diameter	D ( $\pm 0.1/-0$ )	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F ( $\pm 0.05$ )	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 ( $\pm 0.1$ )	2

All dimensions are in mm.

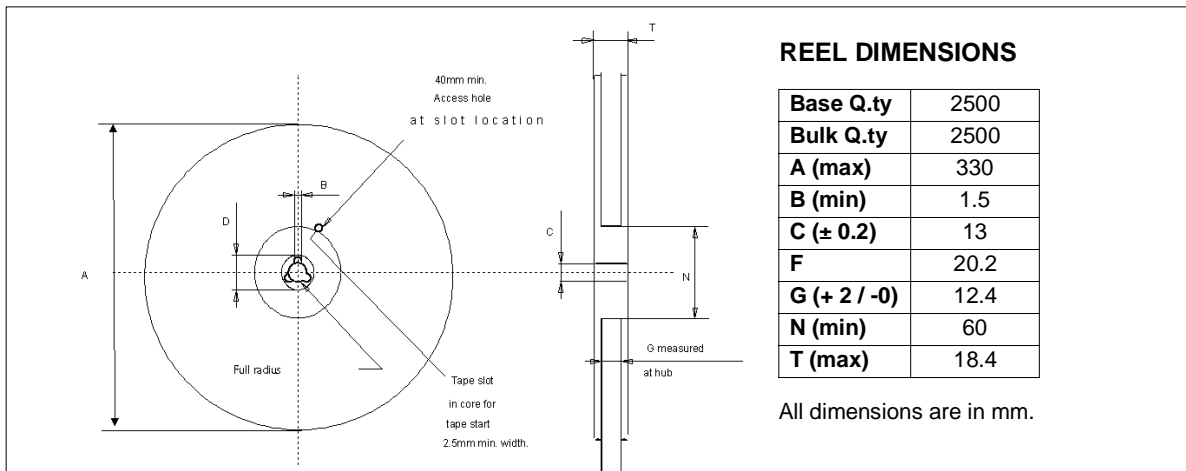


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

SO-8 TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

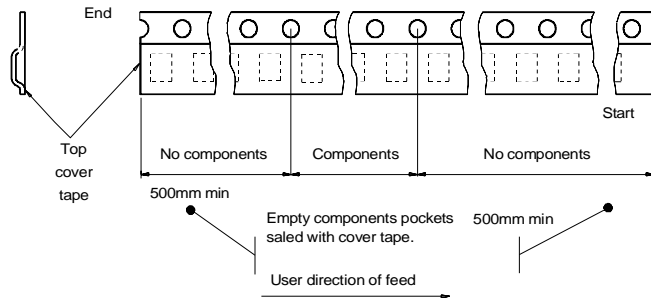
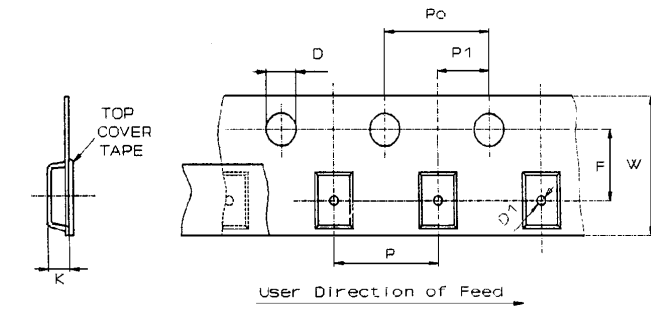
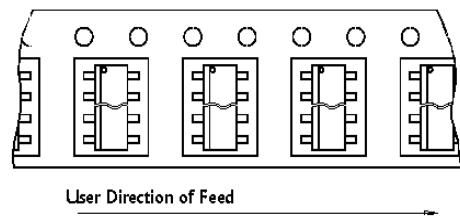


TAPE DIMENSIONS

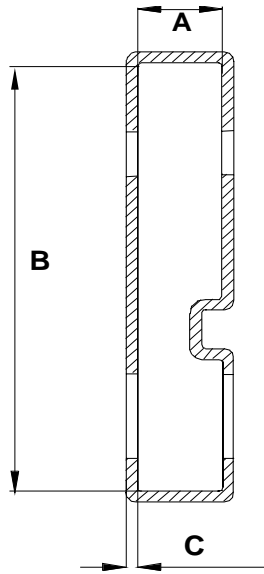
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

<b>Tape width</b>	<b>W</b>	12
<b>Tape Hole Spacing</b>	<b>P0 (± 0.1)</b>	4
<b>Component Spacing</b>	<b>P</b>	8
<b>Hole Diameter</b>	<b>D (± 0.1/-0)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (± 0.05)</b>	5.5
<b>Compartment Depth</b>	<b>K (max)</b>	4.5
<b>Hole Spacing</b>	<b>P1 (± 0.1)</b>	2

All dimensions are in mm.



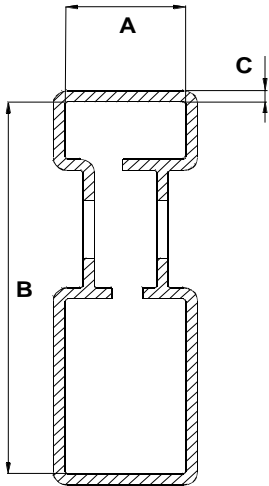
**TO-220 TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	50
<b>Bulk Q.ty</b>	1000
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	5.5
<b>B</b>	31.4
<b>C (<math>\pm 0.1</math>)</b>	0.75

All dimensions are in mm.

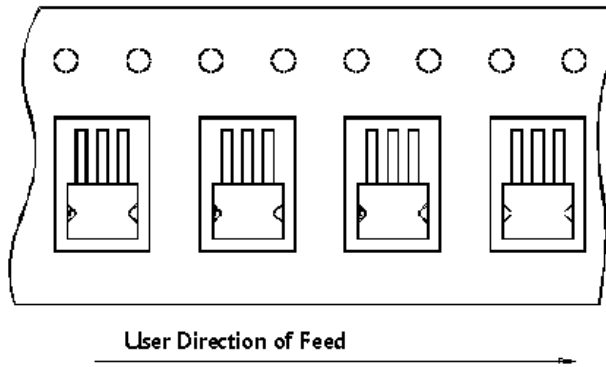
**IPAK TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	75
<b>Bulk Q.ty</b>	3000
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	6
<b>B</b>	21.3
<b>C (<math>\pm 0.1</math>)</b>	0.6

All dimensions are in mm.

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